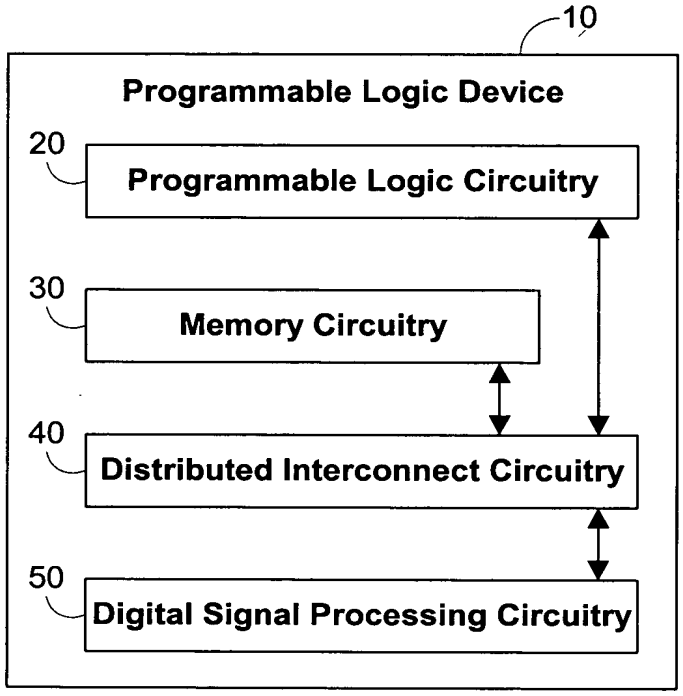
10
Programmable Logic Device
20
Programmable Logic Circuitry
30
Memory Circuitry
40
Distributed Interconnect Circuitry
50
Digital Signal Processing Circuitry

FIG. 1

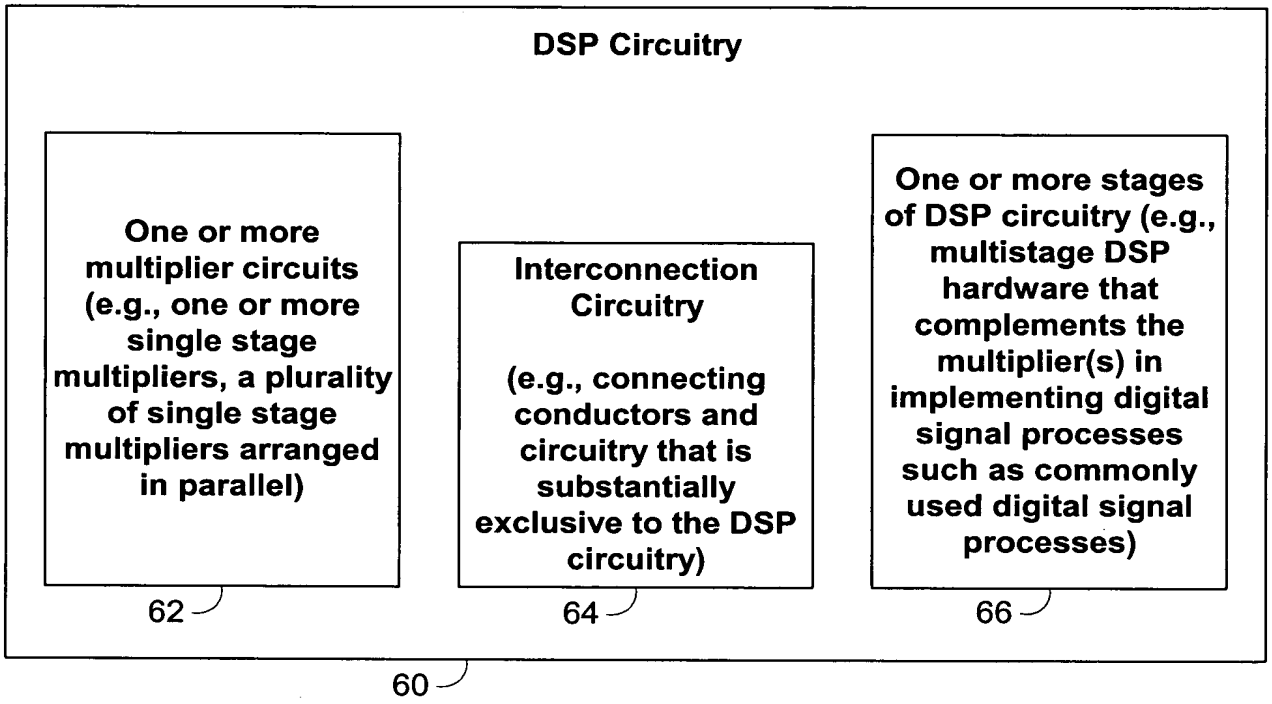
DSP Circuitry
One or more multiplier circuits (e.g., one or more single stage multipliers, a plurality of single stage multipliers arranged in parallel)
62
Interconnection Circuitry
(e.g., connecting conductors and circuitry that is substantially exclusive to the DSP circuitry)
64
One or more stages of DSP circuitry (e.g., multistage DSP hardware that complements the multiplier(s) in implementing digital signal processes such as commonly used digital signal processes)
66
60

FIG. 2

300

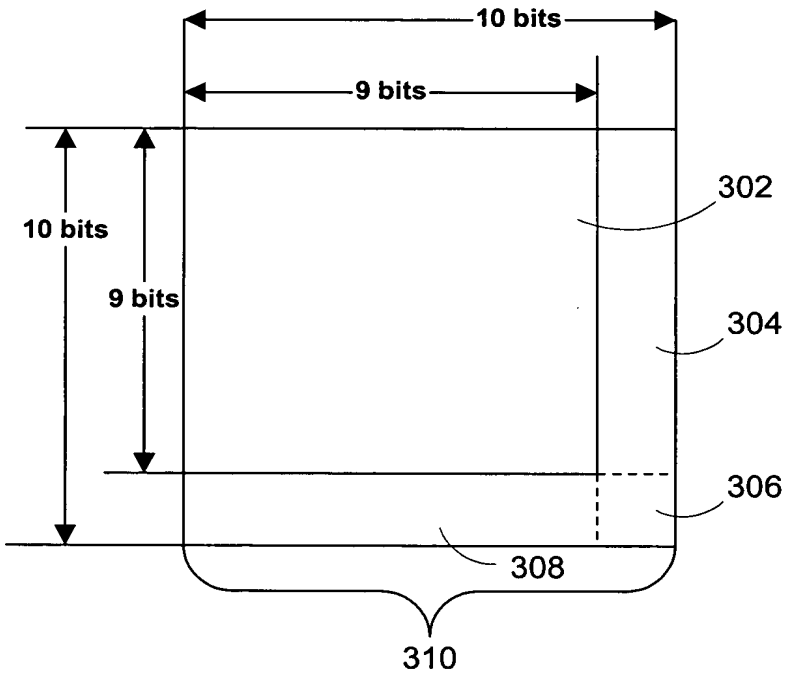

FIG. 3

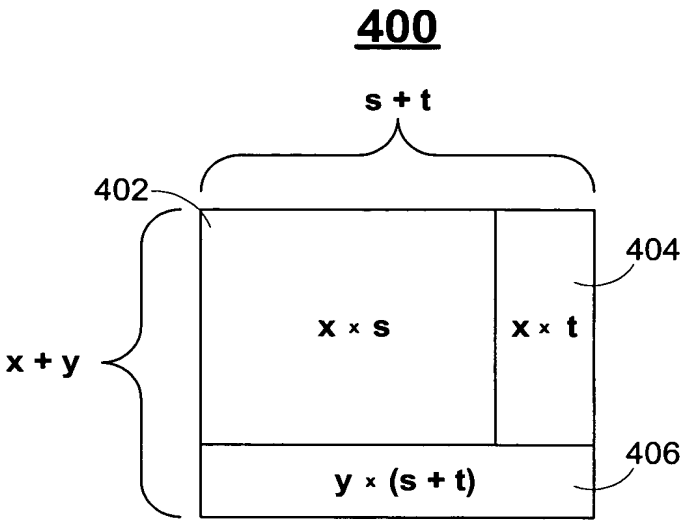
400
s + t
402
404
x × s
x × t
x + y
406
y × (s + t)

FIG. 4

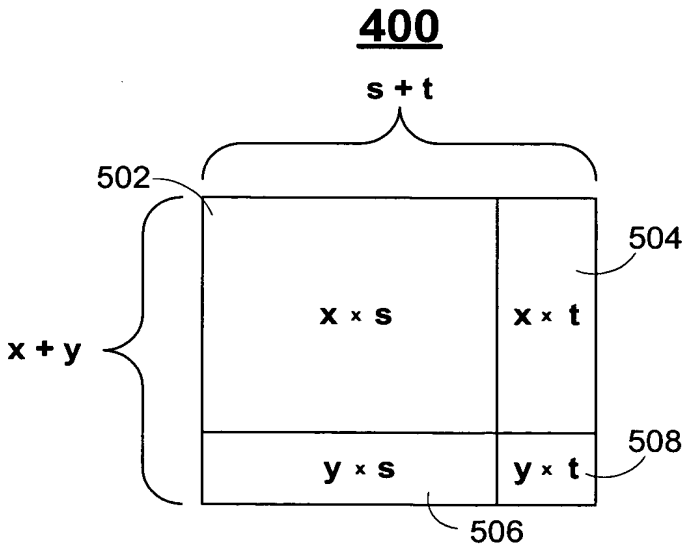
400
s + t
502
504
x × s
x × t
x + y
508
y × s
y × t
506

FIG. 5

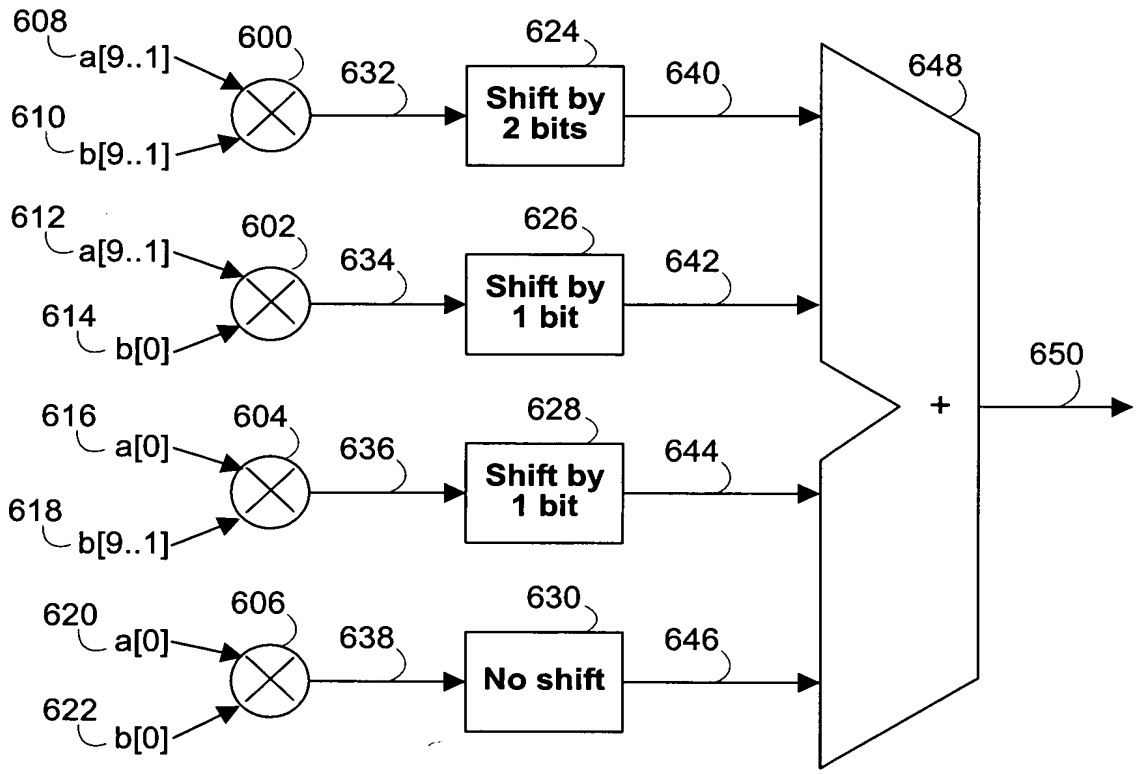
608
a[9..1]
600
632
624
Shift by 2 bits
640
648
610
b[9..1]
612
a[9..1]
602
634
626
Shift by 1 bit
642
614
b[0]
650
+
616
a[0]
604
636
628
Shift by 1 bit
644
618
b[9..1]
620
a[0]
606
638
630
No shift
646
622
b[0]

FIG. 6

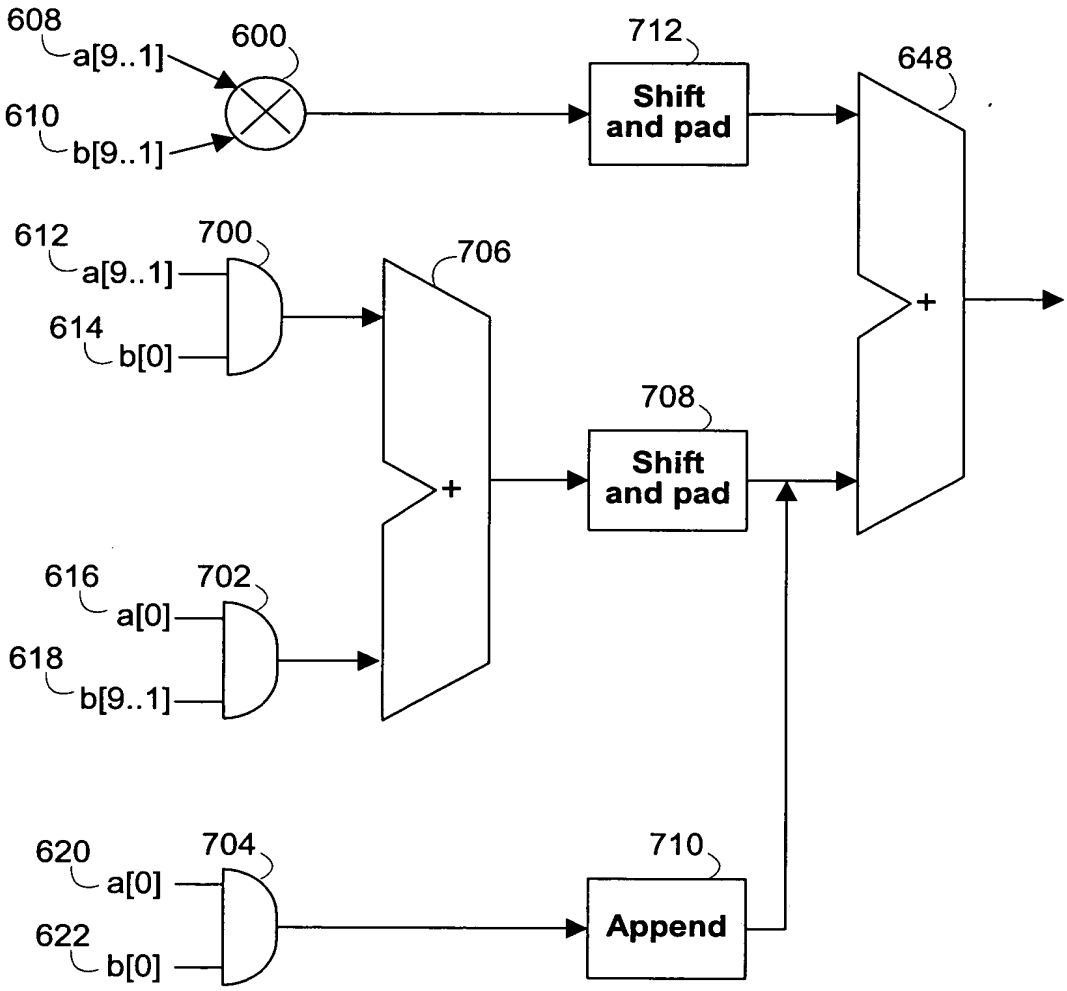
608
a[9..1]
600
610
b[9..1]
712
Shift and pad
648
612
a[9..1]
700
706
614
b[0]
+
708
Shift and pad
616
a[0]
702
618
b[9..1]
620
a[0]
704
710
622
b[0]
Append

FIG. 7

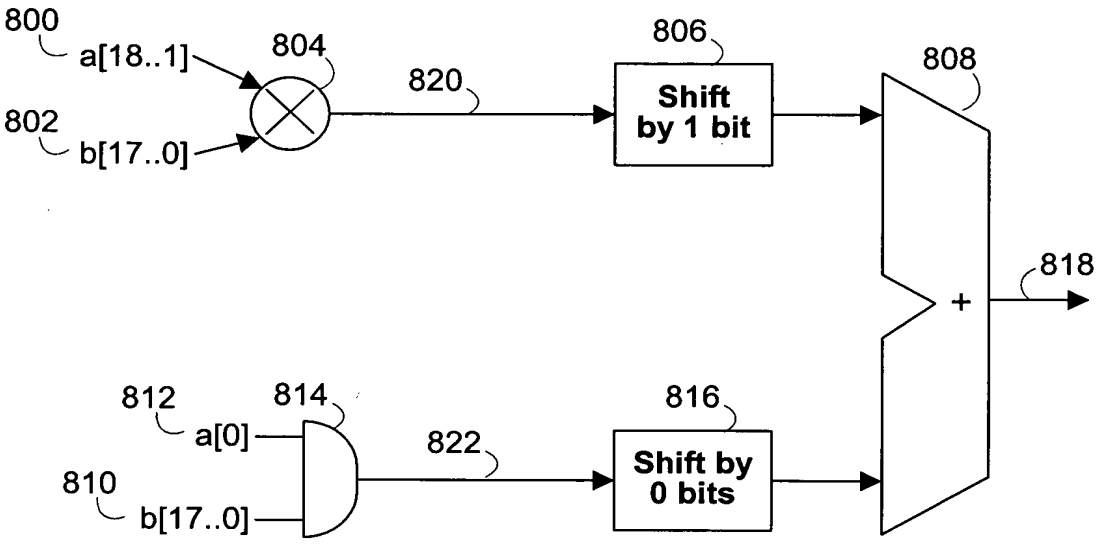
800
a[18..1]
802
b[17..0]
804
820
806
Shift by 1 bit
808
818
+
812
a[0]
810
b[17..0]
814
822
816
Shift by 0 bits

FIG. 8

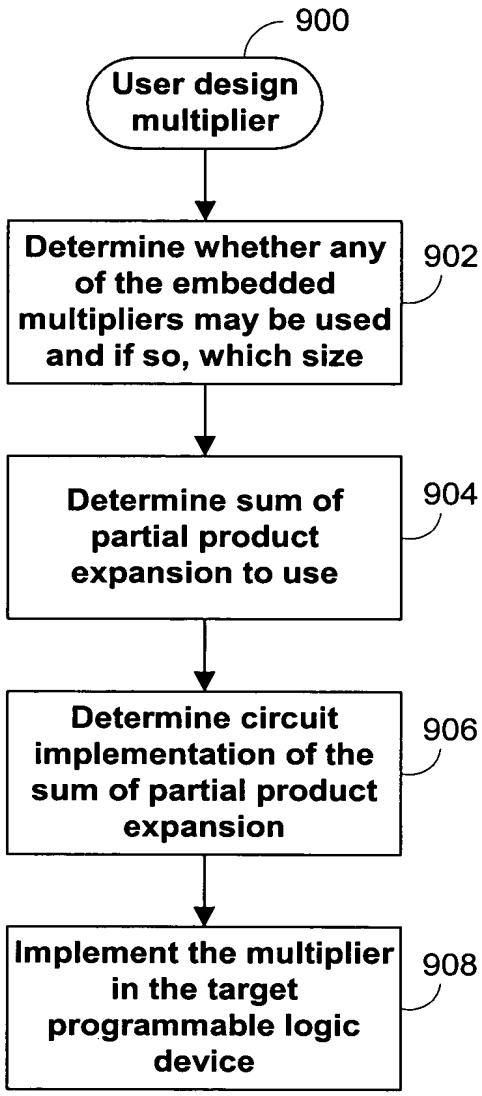
900
User design multiplier
Determine whether any of the embedded multipliers may be used and if so, which size
902
Determine sum of partial product expansion to use
904
Determine circuit implementation of the sum of partial product expansion
906
Implement the multiplier in the target programmable logic device
908

FIG. 9

1000

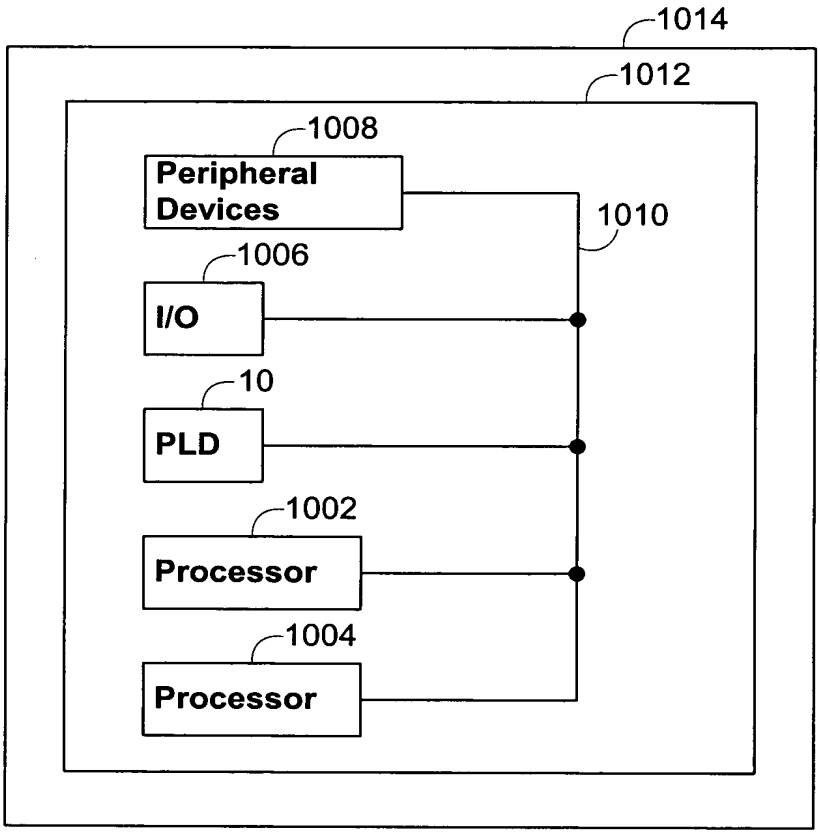
1014
1012
1008
Peripheral Devices
1010
1006
I/O
10
PLD
1002
Processor
1004
Processor

FIG. 10

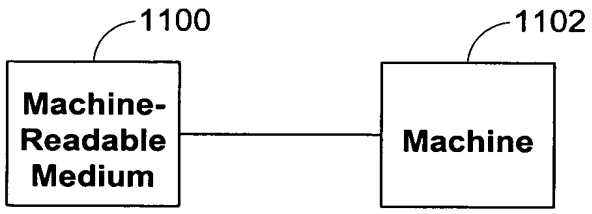

FIG. 11